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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/521,889	05/25/2005	William Robbins	0903-003	8845

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EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
06/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/521,889	ROBBINS ET AL.	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non-Final Office Action

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Popli et al., "A Reconfigurable VLSI Array for Reliability and Yield Enhancement".

Referring to claim 1:

a. In section 4.1, Popli et al. disclose that the complete chip is made up of three elements: a collection of processing elements, a switch lattice, and a controller, and in Figure 3, Popli et al. disclose that the elements are arranged in columns and rows (a processor array comprising a plurality of processor elements arranged in an array of rows and columns, the processor elements being interconnected by buses running between the rows and columns and by switches located at the intersections of the buses).

b. In section 4.1, Popli et al. disclose a spare row and column of redundant PEs (the last row and last column of the array) (and the array including a redundant row to which no functionality is initially allocated).

c. In section 4.2, Popli et al. disclose that the replacement of the faulty PE by the spare PE is achieved by using a sequence of local replacements. The

function of the faulty PE is shifted to its adjacent neighbor, and the function of the adjacent neighbor is moved to its next neighbor, and so on (in the event that a first processor element is found to be faulty, removing functionality from the row that contains said first processing element, and allocating functionality to the redundant row).

Referring to claim 2, in section 4.2, Popli et al. disclose that the replacement of the faulty PE by the spare PE is achieved by using a sequence of local replacements. The function of the faulty PE is shifted to its adjacent neighbor, and the function of the adjacent neighbor is moved to its next neighbor, and so on (allocating the functionality, removed from the row that contains said first processing element, to an adjacent row; and reallocating the functionality from the adjacent row, to a further row adjacent thereto, as required until functionality has been allocated to the redundant row).

Referring to claim 3, in section 4.1, Popli et al. disclose a spare row and column of redundant PEs (the last row and last column of the array) (wherein the redundant row, is located at an edge of the array).

Referring to claims 4 and 9, in section 4.2 and in Figure 4, Popli et al. disclose that in operation of said processor array, data is transferred during time slots between processor elements over horizontal buses running between the rows of processor elements and over vertical buses running between the columns of processor elements, and further comprising: when allocating functionality to the processor elements, such that data is scheduled to be transferred during a first time slot from a first processor element to a second processor element without using any vertical bus, reserving said

time slot for said data transfer on a segment of a vertical bus that would be used in the event of a reallocation of functionality following a determination that either said first processor element or said second processor element were faulty (see reconfiguration algorithm of Popli et al.).

Referring to claim 5:

a. In section 4.1, Popli et al. disclose that the complete chip is made up of three elements: a collection of processing elements, a switch lattice, and a controller, and in Figure 3, Popli et al. disclose that the elements are arranged in columns and rows (a processor array comprising a plurality of processor elements arranged in an array of rows and columns, the processor elements being interconnected by buses running between the rows and columns and by switches located at the intersections of the buses).

b. In section 4.2, Popli et al. disclose that the replacement of the faulty PE by the spare PE is achieved by using a sequence of local replacements. The function of the faulty PE is shifted to its adjacent neighbor, and the function of the adjacent neighbor is moved to its next neighbor, and so on (the method comprising: in the event that a processor element has a fault, allocating no functionality to any processor element in the row containing said processor element).

3. Claims 6-8 are rejected under 35 U.S.C. 102(a) as being anticipated by Claydon, WO 02/50624 A2.

Referring to claim 6:

a. In Figure 1, Claydon discloses a plurality of processor elements arranged in an array of rows and columns, wherein the arrangement of processor elements in each row is the same as the arrangements of processor elements in each other row.

b. On page 7, lines 6-10, Claydon discloses that the architecture includes first bus pairs shown running horizontally, each pair including a first bus carrying data from left to right and a respective second bus carrying data from right to left (pairs of horizontal buses running between the rows of processor elements, each pair comprising a first horizontal bus carrying data in a first direction and a second horizontal bus carrying data in a second direction opposite to the first direction).

c. On page 7, lines 11-15, Claydon discloses that the architecture includes second bus pairs shown running vertically, each pair including a respective third bus shown carrying data upwards and a respective fourth bus shown carrying data downwards (vertical buses running between the columns of processor elements). Further, on page 8, lines 3-5, Claydon discloses that after every four array elements, the horizontal buses are connected to two vertical buses (wherein some pairs of adjacent columns of processor elements have no vertical buses running there between, and other pairs of adjacent columns have two buses carrying data in a first direction and two buses carrying data in a second direction opposite to the first direction running there between).

d. In Figure 1 and on page 7, lines 16-20, Claydon discloses that each diamond connection represents a switch and a switch matrix and each intersection of a first and second bus pair 30, 40 (and switches located at the intersections of the horizontal and vertical buses).

Referring to claim 7:

a. In Figure 2, Claydon discloses that each switch comprises: a plurality of input buses and a plurality of output buses.

b. On page 11, lines 34-37, Claydon discloses that the entire program which an array element executes will be contained in local memory within the array element (a memory device, which stores information at each address thereof, indicating what data is to be switched onto each of the output buses).

c. On page 11, lines 24-26, Claydon discloses that the switches must run a program which is synchronized to the transfer cycles on the buses to which they are connected (and a controller, for counting through addresses of the memory device in a predetermined sequence).

Referring to claim 8, on page 18, lines 20-23, Claydon discloses that array elements execute instructions as a result of receiving data (wherein the memory device stores information which indicates whether the data to be switched onto each of the output buses is: the data value on one of the input buses).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art is related to fault tolerance in processor arrays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571)272-3649. The examiner can normally be reached on M-F 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael C Maskulinski/
Primary Examiner, Art Unit 2113